Japanese Patent Application Laid-Open No. 59-142678

Specification

1. Title of the Invention

FRAME RECOGNITION METHOD

2. Claims for the Patent

(1) A frame recognition method for recognizing a frame by extracting the long line segment in a main scanning direction and a sub-scanning direction on a binary image and discriminating two pairs of long line segments in the main scanning direction and the sub-scanning direction as a frame line, comprising performing a majority decision process for a state of each pixel on each scan line of the binary image with adjacent plural scanning lines, taking a logical sum for the binary image after said majority decision process in the sub-scanning direction on each of plural scanning lines to obtain the binary image reduced in the sub-scanning direction, taking a logical sum for the binary image after said majority decision process in the main scanning direction for each of plural pixels to obtain the binary image reduced in the main scanning direction, extracting the long line segment in the main scanning direction from the binary image reduced in the sub-scanning direction, and extracting the long line segment in the sub-scanning direction from the binary image reduced in the main scanning direction.

3. Detailed Description of the Invention

[Technical Field]

The present invention relates to a method for recognizing the frame on a binary image such as a report or document.

[Conventional Art]

As a method for recognizing the frame on a binary image, there are three representative methods; <1> a method for recognizing the frame by detecting a pattern corresponding to the corner part of the frame through a pattern matching process with a mask, and selecting one of the detected patterns satisfying a predetermined positional relation, <2> a method for recognizing the frame by tracing the line segment, and determining the shape of a locus for the line segment that becomes a closed loop, and <3> a method for recognizing the frame by extracting the long line segment in each of the main scanning and sub-scanning directions and discriminating two pairs of long line segments in each of the main scanning and sub-scanning directions as the frame line.

However, the above method <1> can be applied to the recognition of the frame with clean shape, like the printed frame. However, if it is applied to the recognition of the frame having great variation, like the handwritten frame, the recognition rate is significantly low. That is, there is a drawback that the recognition object has the smaller degree of freedom. The method <2> has a drawback that it is easily susceptible to noise or skew (inclination) such as disconnected line, and requires a relatively large capacity of image buffer, and the processing time is longer.

As the above method <3>, the inventor has already proposed an improved method for making the logical sum process for the binary image in each of the main scanning and sub-scanning directions to reduce the binary image in each of the main scanning and sub-scanning directions, and extracting the long line segment from the reduced image, thereby facilitating the high speed processing without being susceptible to skew (Japanese Patent Application Laid-Open No. 57-104368). However, when a facsimile image is processed, a recognition error may occur. That is, in the transmission image such as the facsimile image, a "black stripe" in the main scanning direction is likely to occur as the noise. If this "black stripe" is falsely extracted as the long line segment, the intrinsic frame may be recognized as segments.

[Object]

It is an object of the invention to provide a frame recognition method that is able to make the high speed processing without requiring a large capacity of image buffer, less susceptible to noise or skew such as a "black stripe", and also applicable to the recognition of a varied frame such as a handwritten frame.

More specifically, the invention provides an improved frame recognition method of the above method <3>.

[Embodiments]

Figure 1 is a schematic block diagram showing one embodiment of the present invention.

A signal of a binary image subject to a frame recognition process is serially inputted into an input terminal 100 pixel by

pixel. This binary image signal is inputted directly into a latch circuit 101, or delayed by a shift register 102, 103 having one line length, and then inputted into a latch circuit 104, 105. Accordingly, the pixel signals (black is "1" and white is "0" in this embodiment) at the same position on three consecutive scanning lines of the binary image are latched by the latch circuits 101, 104, and 105.

An output signal of the latch circuit 101, 104 and 105 is inputted into a majority decision circuit composed of the AND circuits 106, 107 and 108 and an OR circuit 109 to undergo a majority decision process. That is, only if the output signals of two or more of the latch circuits 101, 104 and 105 are "1", the output signal of the OR circuit 109 becomes "1". Though in this embodiment, the majority decision process for three scanning lines is performed, the invention is not limited to this process, but the majority decision for five scanning lines, for example, may be taken. Basically, the number of scanning lines for taking the majority decision can be determined according to the precision of frame recognition. The "black stripe" occurring on the facsimile image has generally a thickness of one pixel and can be removed through the majority decision process.

The output signal of the OR circuit 109 in the majority decision processing circuit and the signals delayed in the shift registers 110 and 111 having one line length are inputted via the latch circuits 127, 128 and 129 into an OR circuit 112 for taking the logical sum. The output signal of this OR circuit 112 is inputted into a counter circuit 113. This counter circuit 113

starts to count pixel clocks, after the input signal transits from "0" to "1", during the enabled interval in a control circuit 114. If the input signal transits from "1" to "0", the counter circuit 113 outputs a count value and is reset. That is, the output signal of the OR circuit 112 becomes effective only during the interval where the counter circuit 113 is enabled by the control circuit 114. Referring to Figure 2, this timing control will be described below.

In Figure 2, $S_{i,j}$ denotes a pixel on the input binary image, where i is the address (scanning line number) in the sub-scanning direction and j is the address in the main scanning direction. The positions of pixels before the majority decision process correspond one to one to the positions of pixels after the majority decision process (i.e., no reduction is made). The control circuit 114 enables the counter circuit 113 for one scanning line interval to make the output signal of the OR circuit 112 effective from the time when the majority decision processing signals of the scanning lines with i = 0 and i = 1 are accumulated in the shift register 110, 111 and the majority decision processing signal with i = 2 is outputted from the majority decision processing OR circuit 109. Similarly, it makes the output signal of the OR circuit 112 effective on the last scanning line (i = 5) of the next three scanning lines. Under the same control, the majority decision processed image is substantially blocked for every three scanning lines, and three scanning lines of each block are ORed in the sub-scanning direction, and reduced into the one scanning line. In this manner, the pixel on the image reduced into 1/3 in the sub-

scanning direction is $V_{I,j}$ in Figure 2, where I is the address in the sub-scanning direction and j is the address in the main scanning direction. j of $V_{I,j}$ corresponds one to one to $S_{i,j}$, in which I = 0 corresponds to i = 0 to 2, and I = 1 corresponds to i = 3 to 4.

The reduction ratio is not limited to 1/3.

Turning back to Figure 1, the counter circuit 113 counts the length (run length) of black run on each scanning line of image reduced in the sub-scanning direction and outputs it, as will be apparent from the previous description. A comparison circuit 115 compares the run length outputted from the counter circuit 113 with a predetermined value $l_M$. If the run length is $l_M$ or greater, a write signal is sent to a length memory 116 and a position memory 117. The length memory 116 stores internally data of run length outputted from the counter circuit 113 upon receiving the write signal. Also, the address I,j of the reduced image from the control circuit 114 is inputted into the position memory 117, and data of the address I,j when the write signal is given is internally stored in the position memory 117. That is, the majority decision process is performed for the input binary image, and run length data of a black run having the run length of $l_M$ or greater among the black runs on the image reduced in the sub-scanning direction through the logical sum process and the address data at the end (right end) of the black run are acquired in the length memory 116 and the position memory 117.

Reference numeral 118 denotes an integration circuit for integrating the black runs that can be regarded as one long line segment among the black runs in the main scanning direction

extracted in the above manner by referring to data stored in the length memory 116 and the position memory 117. That is, the black run with I = k and the other black run with I = k or I = k±1 is integrated into one black run, if the mutual distance in the main scanning direction between the trailing edge and the leading edge or the leading edge and the trailing edge is smaller than or equal to a certain value m. The leading edge address of the black run is known from the trailing edge address and the run length. For example, one pair of black runs as shown in Figures 3A, 3B and 3C are integrated. And the integration circuit 118 acquires the addresses of the integrated black run, namely, the leading edge and the trailing edge of the long line segment in the main scanning direction, and outputs them.

In this manner, since the black runs extracted from the image reduced by the logical sum are integrated to extract the long line segment in the main scanning direction, the long line segment inclined as a whole due to skew, locally interrupted due to noise, changed in the line width, or somewhat curved such as the handwritten frame can be securely extracted. And since the "black stripe" is removed through the majority decision process as previously described, it does not occur that the "black stripe" is extracted falsely as the long line segment.

The extraction of the long line segment in the sub-scanning direction is similarly performed, and will be described below.

The output signal of the OR circuit 109 in the majority decision circuit is inputted sequentially into an 8-bit shift register 119, and every time 8 pixels are accumulated, the output timing from the control circuit 114 is sent. The shift

register 119 outputs the contents in parallel, and then is reset. The output signal of this shift register 119 is ORed in an OR circuit 120, so that an image signal reduced to 1/3 in the main scanning direction is inputted into a counter memory circuit 121.

In Figure 2, $H_{i,j}$ denotes a pixel on the image reduced in the main scanning direction, where i corresponds one to one to i of $S_{i,j}$, and J = 0 corresponds to j = 0 to 2 of $S_{i,j}$, and J = 1 corresponds to j = 3 to 5.

The reduction ratio is not limited to 1/3.

Turning back to Figure 1, the counter memory circuit 121 has a counter function and a function as a memory having the memory address equivalent to the maximum value of address J. That is, when the value of address J given from the control circuit 114 is changed (at this time, the content of the shift register 119 is outputted), the counter memory circuit 121 adds 1 to the storage content at the memory address (J), if the output signal of the OR circuit 120 is "1". Also, if the output signal of the OR circuit 120 is "0", the storage content at the memory address (J) is outputted, and then the storage content at the same memory address is cleared. That is, the counter memory circuit 121 is the circuit that extracts the black run in the sub-scanning direction on the image reduced in the main scanning direction to obtain its run length, and outputs its run length if the trailing edge (lower edge) of the black run is detected.

A comparison circuit 122 compares the run length outputted from the counter memory circuit 121 with a certain value $l_v$. If the run length is $l_v$ or greater, a write signal is sent. If this write signal is sent, a length memory 123 stores internally the

run length data outputted from the counter memory circuit 121. Also, a position memory 124 stores data at the address i,J given from the control circuit 114, if the write signal is outputted. An integration circuit 125 is the circuit, like the integration circuit 118, for making the integration process for the extracted black runs in the sub-scanning direction by referring to the stored data in the length memory 123 and the position memory 124. That is, the black run with J = k and the other black run with J = k or J = k±1 is integrated into one black run, if the mutual distance in the sub-scanning direction between the trailing edge and the leading edge or the leading edge and the trailing edge is smaller than or equal to a certain value. The addresses of the leading edge and trailing edge of the integrated black run (long line segment in the sub-scanning direction) are outputted.

In this manner, since the black runs extracted from the image reduced by the logical sum are integrated to extract the long line segment in the sub-scanning direction, the long line segment inclined as a whole due to skew, locally interrupted due to noise, changed in the line width, or somewhat curved such as the frame line of handwritten frame can be securely extracted.

The long line segments in the main scanning and sub-scanning directions extracted in the above manner are candidates for the frame line, and each data is inputted into a frame recognition part 126. This frame recognition part 126 recognizes the area of the frame by checking the relative position relationship of the long line segment as the frame line candidate to be inputted and discriminating one pair of long line segments in the main

scanning direction and one pair of long line segments in the sub-scanning direction that make up one frame. This process for frame recognition is performed through the same procedure as detailed in Japanese Patent Application Laid-Open No. 57-104368, and is not the gist of the invention, whereby the detailed explanation thereof is omitted.

[Advantages of the Invention]

As detailed above, with the invention, since the long line segment as the frame line candidate is extracted from the image reduced by the logical sum in each of the main scanning and sub-scanning directions after the majority decision process, the frame recognition method is less susceptible to skew or noise such as "black stripe", and can recognize securely not only the printed frame but also the irregular shape such as a handwritten frame, whereby there is the effect that the high speed processing can be easily achieved without using a large capacity of image buffer, as will be apparent from the above embodiment.

4. Brief Description of the Drawings

Figure 1 is a schematic block diagram showing one embodiment of the present invention;

Figure 2 is a view for explaining the reduction of an image; and

Figure 3 is a view showing an example of integrated line segment.

102, 103, 110, 111, 119 ... shift registers

101, 104, 105, 127, 128, 129 ... latch circuits

118 ... counter circuit

114 ... control circuit

115, 122 ... comparison circuits

116, 128 ... length memories

117, 124 ... positional memories

118, 125 ... integration circuits

121 ... counter memory circuit

126 ... frame recognition part

Figure 1

100 Image input

101 Latch

102 Shift register

103 Shift register

104 Latch

105 Latch

110 Shift register

111 Shift register

113 Counter circuit

114 Control circuit

115 Comparison circuit

116 Length memory

117 Position memory

118 Integration circuit

119 Shift register

121 Counter memory circuit

122 Comparison circuit

123 Length memory

124 Position memory

125 Integration circuit

126 Frame recognition part

127 Latch

128 Latch

129 Latch